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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Suraj J. Mathew et al.

Title: METHOD TO FABRICATE SURFACE P-CHANNEL CMOS

Docket No.: 303.744US1

Serial No.: 09/808,261

Filed: March 14, 2001

Due Date: January 3, 2003

Examiner: Christopher Lattin

Group Art Unit: 2812


Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

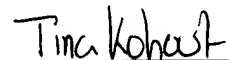
- ☒ A return postcard.
- ☒ An Amendment and Response (6 Pages).
- ☒ A Clean Version of Pending Claims (12 pgs.).

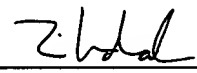
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 19 day of December, 2002.


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S/N 09/808,261

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

Applicant: Suraj J. Mathew et al.

Examiner: Christopher Lattin

Serial No.: 09/808,261

Group Art Unit: 281

Filed: March 14, 2001

Docket: 303.744US1

Title: METHOD TO FABRICATE SURFACE P-CHANNEL CMOS

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
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Applicant has reviewed the Office Action mailed on October 3, 2002. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 6, 13, and 18. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) A method of forming a transistor, comprising:
 - forming a gate dielectric layer on a semiconductor substrate;
 - forming a first conductivity type semiconductor layer on top of the gate dielectric layer;
 - selectively removing a portion of the first conductivity type semiconductor layer to expose the gate dielectric, the portion defining a first conductivity type well region;
 - forming a first conductivity type semiconductor well in the first conductivity type well region;
 - modifying the gate dielectric layer in the first conductivity type well region, the modified gate dielectric being adapted for operation with a second conductivity type gate material;
 - depositing a second conductivity type semiconductor material on the modified gate dielectric layer and forming a second conductivity type gate from the second conductivity type semiconductor layer; and
 - forming source/drain regions adjacent the gate.